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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,370	04/09/2004	Anders Landin	5181-99901	1207

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EXAMINER	
ELAND, SHAWN	
ART UNIT	**PAPER NUMBER**
2188	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/22/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/821,370	LANDIN ET AL.	
	Examiner	Art Unit	
	Shawn Eland	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2004, 11 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07/11/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claims 6 & 32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 32 depends upon claim 14, which is claimed as a node by claim 32, but is actually a system. For the purposes of applying art, the Examiner will assume that claim 32 really depends upon claim 29.

Claim 6 recites the limitation "the active device" in page 133, line 3. There is insufficient antecedent basis for this limitation in the claim. It is not clear which of the 2 listed active devices is referred to in this claim. For the purposes of applying art, the Examiner will assume this to mean either active device.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 – 48 are rejected under 35 U.S.C. 102(b) as being anticipated by ***Liencres et al.*** (US 5,434,993).

In regards to claim 1, Liencres teaches a node ***(see element 20)*** including an active device ***(see element 21)***, an interface to an inter-node network ***(see element 31)***, a memory ***(see element 37)***, and an address network coupling the active device, the interface, and the memory **(see element 33)**; an additional node coupled to the node by the inter-node network ***(see figure 3a; see column 6, lines 11 - 15)***; wherein in response to receiving from the active device an address packet initiating a transaction to gain an access right to a coherency unit, the memory is configured to send data corresponding to the coherency unit to the active device dependent on memory response information associated with the coherency unit ***(see column 7, "Read Transactions")***; wherein if the transaction cannot be satisfied within the node, the memory is configured to forward a report corresponding to the address packet to the interface, wherein in response to the report, the interface is configured to send the additional node a coherency message requesting the access right via the inter-node network ***(see column 7, "Read Transactions")***.

In regards to claim 17, Liencres teaches a plurality of devices including a memory ***(see element 37)***, an active device ***(see element 21)***, and an interface to an inter-node network coupling nodes in the multi-node computer system ***(see element 31)***; an address network configured to convey packets between the plurality of devices ***(see element 33)***; wherein in response to receiving from the active device an address packet initiating a transaction to gain an access right to a coherency unit, the memory is

configured to send data corresponding to the coherency unit to the active device dependent on memory response information associated with the coherency unit ***(see column 7, "Read Transactions")***; wherein if the transaction cannot be satisfied within the node, the memory is configured to forward a report corresponding to the address packet to the interface, wherein in response to the report, the interface is configured to send a coherency message requesting the access right to another one of the nodes via the inter-node network ***(see column 7, "Read Transactions")***.

In regards to claim 33, Liencres teaches an active device ***(see element 21)*** included in the node initiating a transaction to gain an access right to a coherency unit by sending an address packet on an address network included in the node ***(see column 7, "Read Transactions")***; dependent on memory response information associated with the coherency unit, a memory included in the node sending data corresponding to the coherency unit to the active device in response to the address packet ***(see column 7, "Read Transactions"; if the node owns the coherency unit, there is no need to look for the data on other nodes)***; if the transaction cannot be satisfied within the node, the memory forwarding a report corresponding to the address packet to the interface; in response to the report, the interface sending the additional node a coherency message requesting the access right via the inter-node network ***(see column 7, "Read Transactions")***.

For claims 2 & 18, Liencres teaches a data network coupling the active device, the interface, and the memory, and wherein the memory is configured to send the report to the interface in a data packet ***(see element 33)***.

For claim 34, Liencres teaches wherein said forwarding the report comprises the memory send a data packet including the report to the interface via a data network included in the node ***(see element 33)***.

For claims 3, 19, & 35, Lawrence teaches wherein the memory response information is configured to identify one of at least two possible response states ***(see column 7, "Read Transactions", last sentence; see column 1, lines 64 - 65)***.

For claims 4, 20, & 36, Liencres teaches wherein if the memory response information indicates a no response state, the memory is configured to send neither the data nor the report in response to the address packet; wherein when the memory response information indicates the no response state, an additional active device ***(see element 35)*** included in the node has an ownership responsibility for the coherency unit and is configured to supply the data to the active device in response to receiving the address packet ***(see column 7, "Read Transactions")***.

For claims 5 & 21, Liencres teaches wherein if the address packet is conveyed in point-to-point mode by the address network ***(see element 33 in figure 3a; having only 2 processors would, in effect, be a point-to-point mode)***, the memory is configured to send an additional address packet indicating the transaction to the additional active device having the ownership responsibility for the coherency unit ***(see column 7, "Read Transactions", 1st paragraph; the processor cache memory 37 indicates to the processor cache controller 35 that the memory request cannot be fulfilled)***.

For claim 37, Liencres teaches the memory sending an additional address packet indicating the transaction to the additional active device having the ownership

responsibility for the coherency unit ***(see column 7, "Read Transactions", 1st paragraph; the processor cache memory 37 indicates to the processor cache controller 35 that the memory request cannot be fulfilled)*** if the address packet is conveyed in point-to-point mode by the address network ***(see element 33 in figure 3a; having only 2 processors would, in effect, be a point-to-point mode)***.

For claims 6 & 22, Liencres teaches wherein the memory is configured to update the memory response information to indicate the no response state in response to receiving the address packet, and wherein the active device is configured to gain an ownership responsibility for the address packet in response to receiving the address packet ***(see figure 1c; if there's no response, then the processor will take the data from main memory and subsequently "own" it until it does a write-back)***.

For claim 38, Liencres teaches the memory updating the memory response information to indicate the no response state in response to receiving the address packet; and the active device gaining an ownership responsibility for the address packet in response to receiving the address packet ***(see figure 1c; if there's no response, then the processor will take the data from main memory and subsequently "own" it until it does a write-back)***.

For claims 7 & 23, Liencres teaches wherein the memory is configured to update the memory response information to indicate a response state in response to receiving an address packet providing the memory with an ownership responsibility for the coherency unit; wherein if the memory response information identifies the response state, the memory is configured to send the data corresponding to the coherency unit to

the active device in response to the address packet ***(see column 7, "Read Transactions"; see figure 1c; if the data does not exist in cache, it will be owned by the node)***.

For claim 39, Liencres teaches the memory updating the memory response information to indicate a response state in response to receiving an address packet providing the memory with an ownership responsibility for the coherency unit; wherein if the memory response information identifies the response state, the memory sends the data corresponding to the coherency unit to the active device in response to the address packet ***(see column 7, "Read Transactions"; see figure 1c; if the data does not exist in cache, it will be owned by the node)***.

For claims 8, 24, & 40, Liencres teaches wherein if the memory response information indicates a shared response state, the memory is configured to not send the report and to send the data corresponding to the coherency unit if the access right is a read access right ***(see column 7, "Read Transactions")***; wherein if the memory response information indicates the shared response state and the access right is a write access right, the memory is configured to not send the data to the active device and to send the report to the interface ***(see column 7, "Write Transaction")***.

For claims 9, 25, & 41, Liencres teaches wherein the memory is configured to update the response information to indicate the shared response state in response to a proxy address packet sent by the interface indicating that an additional active device in the additional node is requesting read access to the coherency unit ***(see column 7, "Read Transactions"; according to [00189] in the applicant's specification, proxy***

packets are packets sent by the interface 148; the processor cache controller 35 and the interface 148 are one and the same).

For claims 10, 26, & 42, Liencres teaches wherein if the memory response information indicates an invalid response state, the memory is configured to not send the data to the active device and to send the report to the interface in response to the address packet ***(see column 7, "Read Transactions"; see column 1, lines 64 - 67)***.

For claims 11, 27, & 43, Liencres teaches wherein the memory is configured to update the memory response information to indicate the invalid response state in response to receiving a proxy address packet from the interface indicating that an additional active device included in the additional node is requesting write access to the coherency unit ***(see column 1, lines 64 – 68 through column 2, lines 1 – 4)***.

For claims 12, 28, & 44, Liencres teaches wherein the memory is configured to send the data dependent on both the memory response information and a global access state of the coherency unit within the node, wherein the memory is configured to send the report dependent on the global access state ***(see column 7, "Read Transactions"; see column 1, lines 64 – 68 through column 2, lines 1 – 12)***.

For claims 13, 29, & 45, Liencres teaches wherein the memory is configured to include a value of the memory response information in the report, wherein the value is a value of the memory response information before the memory response information is modified in response to the address packet ***(see column 1, lines 64 - 65)***.

For claims 14 & 30, Liencres teaches wherein the interface is configured to maintain a plurality of records in an outstanding transaction queue, wherein each of the

plurality of records corresponds to a respective report received from the memory, and wherein the interface is configured to determine a global access state of the coherency unit in the node from the value of the memory response information included in the report and from one or more of the records in the outstanding transaction queue ***(see element 40; see column 9, lines 32 – 47)***.

For claim 46, Liencres teaches the interface maintaining a plurality of records in an outstanding transaction queue, wherein each of the plurality of records corresponds to a respective report received from the memory; and the interface determining a global access state of the coherency unit in the node from the value of the memory response information included in the report and from one or more of the records in the outstanding transaction queue ***(see element 40; see column 9, lines 32 – 47)***.

For claim 15, Liencres teaches in response to receiving an additional coherency message specifying the coherency unit from the additional node, the interface is configured to select a type of proxy address packet to send on the address network dependent on the global access state ***(see column 8, lines 56 – 62)***.

For claim 31, Liencres teaches in response to receiving an additional coherency message specifying the coherency unit from another node, the interface is configured to select a type of proxy address packet to send on the address network dependent on the global access state ***(see column 8, lines 56 – 62)***.

For claim 47, Liencres teaches in response to receiving an additional coherency message specifying the coherency unit from the additional node, the interface selecting

a type of proxy address packet to send on the address network dependent on the global access state ***(see column 8, lines 56 – 62)***.

For claims 16 & 32, Liencres teaches if the memory subsequently updates the memory response information again in response to another address packet, the memory is configured to provide a new value of the memory response information to the interface ***(see column 9, lines 1 – 8)***.

For claim 48, Liencres teaches if the memory subsequently updates the memory response information again in response to another address packet, the memory providing a new value of the memory response information to the interface ***(see column 9, lines 1 – 8)***.

Examiner Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Eland whose telephone number is (571) 270-1029. The examiner can normally be reached on Monday - Thursday from 7:30am to 5:00pm. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough, can be reached on (571) 272-4199. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shawn Eland
12/20/2006

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER
12/21/06